Remarks

Claims 1-10 are pending in this action. Claims 1-10 stand rejected. By this amendment claims 1, 5-7 and 10 have been amended. Applicants respectfully request reconsideration of all pending claims herein.

Response To Arguments

The Examiner indicated that the features on which Applicant relies to distinguish the invention herein from the references cited are not recited in the rejected claims and noted that limitations from the specification will not be read into the claims. Applicants have amended independent claims 1 and 10 in the response to the previous Office Action and have also amended claims 5-7 to correct a repeated deficiency in grammar.

Accordingly, claim 1 has been amended to include imitations directed to providing a test fixture capable of coupling a plurality of banked I/O pins to a tester and modifying the I/O test patterns such that more than one set of stimuli may be applied to an external I/O pin.

Similarly, claim 10 has been amended to include a limitation directed to assigning a single tester channel to a banked set of device I/O, which is not taught or suggested by Ellison or Godiwala. In addition, claim 10 has been amended to include a limitation directed to the generation of testing patterns after the integrated circuit to be tested is designed and manufactured, which is not taught or suggested by the references cited.

Claim Rejections - 35 U.S.C. § 103(a)

The Examiner rejected claims 1-8 under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 6,448,796 issued to Ellison, et al. in view of U.S. Patent No. 5,348,759 issued to Schnurmann, et al. The Examiner also rejected claim 10 under 35 U.S.C. § 103(a), as being unpatentable over U.S. Patent No. 6,448,796 issued to Ellison, et al. in view of U.S. Patent No. 5,712,858 issued to Godiwala.

With respect to the rejection of claim 1, the Examiner stated that it would have been obvious to one of ordinary skill in the art to implement a method of parametric testing of high pin count circuits with low channel testers, citing Ellsion in view of Schnurman.

Applicants respectfully submit that U.S. Patent No. 6,448,796 issued to Ellison, et al. is directed to a method of grouping I/O pins of common types of module drivers to a particular channel of an integrated circuit tester to reduce the incidence of shorts between adjacent pins. Ellison requires a circuit designer to "insert logic driver controls in the design to allow only a **single** group driver of a grouping bank to be active for any given test vector." (Col. 3, lines 63-65) Moreover, the logic control elements of Ellison must be designed for each individual integrated circuit design that is tested. (Col. 3, lines 66-67 through Col. 4, lines 1-9) Conversely, Applicants' invention does not require the custom design of logic controls that are specific to each design and is therefore not suggested or motivated by Ellison. The data to configure the tester channels such that more than one stimulus can be applied per test pattern on external I/O circuits is derived from a design-specific Test Manufacturing Data (TDM) file generated prior to manufacture of the device under test and an I/O pin banking configuration implemented in a module test fixture that is designed and manufactured once the physical I/O pin mapping and chip module substrate definitions are known. (Applicants' Spec. Paragraphs. 13, 30 and 36) In this regard, Applicants construct a unique testing configuration using the test patterns contained within the TDM file together with the definition for banked pin groups such that no additional logic is needed on the device under test to implement full pin count testing on a reduced pin-count tester. (Applicants' Spec. Paragraphs 30, 36)

Applicants further submit that Schnurman teaches a method whereby a plurality of terminal pins are connected to a single channel, such that each test pattern forces a logic 0 or 1 to every input pin, which necessarily requires **each pin** to receive the same set of stimuli. (Col. 6, lines 24-32; Col. 8, lines 16-22) In contrast, Applicants' invention does not connect multiple pins of the device under test to a single tester channel. Instead, Applicants' invention permits more than one stimulus per test pattern on the external I/O pins through repeated simulation by muxing different test

vectors to the same tester channel and performing multiple simulations. (Applicants' Spec. Paragraphs. 23, 39) Any and all of the pins in the active bank can have stimuli applied by one of the re-simulated test patterns. (Applicants' Spec. Paragraphs. 39, 51 and 57) Accordingly, Applicants' invention is not suggested or motivated by Schnurman.

As noted above, Applicants have amended claim 1 to incorporate limitations cited in the specification that patentably distinguish the references cited by the Examiner. Therefore, Applicants respectfully submit that the rejection of claim 1 under 35 U.S.C. §103(a) has been overcome and that claim 1 is in condition for allowance. Applicants have also amended claims 5-7 to correct further deficiencies in grammar. Claims 2-9 depend on claim 1, as amended. Therefore, Applicants respectfully submit that the rejection of claims 1-8 under 35 U.S.C. § 103(a) has been overcome and claims 1-9 are in condition for allowance.

In regard to the rejection of claim 10, the Examiner cited Ellison in view of Godiwala, stating that it would have been obvious to a person of ordinary skill in the art, at the time of invention, to combine the method of parametric testing claimed by Ellison with the testing system of Godiwala. The Examiner noted that Godiwala teaches connecting the contacts to the tester such that groups of contacts share individual tester channels. Conversely, Applicants invention discloses that for each test of a banked set of device I/O, the device I/O are assigned a single tester channel. Since Applicants do not utilize a parallel test of common device I/O, the individual failing devices can be isolated by the tests. In addition, Applicants note that the parametric tests performed in accordance with Applicants' invention may be constructed after a design is completed and the devices are fabricated, which is clearly not contemplated by the art cited. (Applicants' Spec. Paragraphs 36, 39) Indeed, Ellison and Godiwala both require custom logic to be incorporated in the design of the integrated circuit under test to support their respective test methodologies. (Ellison, Col 3, lines 66-67 through Col. 4, lines 1-9; Godiwala, Col. 5, lines 26-34, Fig. 2) Accordingly, Applicants respectfully submit that the flexibility of Applicants' test methodology is not suggested or motivated by Ellison or Godiwala.

As noted above, Applicants have amended claim 10 to incorporate limitations cited in the specification that patentably distinguish the references cited by the Examiner. Accordingly, Applicants respectfully submit that the rejection of claim 10 under 35 U.S.C. § 103(a) has been overcome and all claims are in condition for allowance.

Prior Art Made of Record

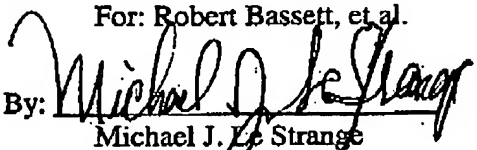
The prior art made of record by the Examiner and not relied upon, i.e. Rearick (U.S. Patent No. 6,658,613); Rohrbaugh, et al. (U.S. Patent No. 6,556,938); Littlebury (EP Patent No. 0388790 A2); and Chang, J.M. (Inspec Accession No. 3976214), has been reviewed and Applicants respectfully submit that the references cited do not anticipate or suggest the elements of pending independent claim 1 and independent claim 10, as amended.

Conclusion

Based on the foregoing, it is respectfully submitted that the pending claims in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Robert Bassett, et al.

By: 

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